AMENDMENTS TO THE DRAWINGS

Attached hereto are two (2) sheets of corrected formal drawings that comply with the provisions of 37 C.F.R. § 1.84. The corrected formal drawings incorporate the following drawing changes:

In Fig. 2, previously omitted nodes have been added, and the gates of two PMOS and one NMOS in the driving circuit have been amended to be connected with each other; and

In Fig. 3, previously omitted nodes have been added, the gates of two PMOS and one NMOS in the driving circuit have been amended to be connected with each other, and the label "N1" has been amended to relate to the diode string 441 in the voltage detecting device 44.

It is respectfully requested that the corrected formal drawings be approved and made a part of the record of the above-identified application.